2012 IEEE NORTH ATLANTIC TEST WORKSHOP
MAY 9-11, HOLIDAY INN SELECT, WOBURN MA

The IEEE North Atlantic Test Workshop provides a forum for discussions on the latest issues relating to high quality, economical, and efficient test methodologies and designs. In addition to traditional topics, the 21st NATW will feature test in 3D and die stacking with a theme of "*Test Challenges in Mobile Computing.*"

This year's NATW includes 21 papers from 4 different companies and 8 different universities, including 10 student papers competing for the **Jake Karrfalt Best Student Paper Award**. In addition, the workshop includes a Keynote Address on "Opportunities and Challenges in the Design and Test of Post-CMOS Memories" by Dr. Fabrizio Lombardi from Northeastern University, a 1st Invited Address on "Data Analytics and Applications for End-to-End Optimization" by Matthias Kamm from Cisco Systems, an IEEE Women in Engineering informational session, and a 2nd Keynote Address on "Timing Tests in the Face of Random Transistor Performance Variability" by Professor Adit Singh from Auburn University. The 2012 workshop is being held at the Holiday Inn Select in Woburn, MA and is sponsored, in part, by the Green Mountain and Boston sections of IEEE. It is organized in cooperation with TTTC and the IEEE Boston Section. NATW corporate and academic supporters for 2012 include Mentor Graphics, SynTest Technologies, Cadence, Amkor, AdamsIP, Maxim, the Wireless Engineering Research and Education Center at Auburn University, IEEE Women in Engineering, and the Vermont chapter of the IEEE Solid State Circuits Society.

Wednesday, May 9	
12:00	**Registration**
12:30-4:30	**Invited Tutorial:** "Testing of 3-D Stacking Devices"**,** Prof. Krishnendu Chakrabarty, Duke University
7:30-9:00 pm	**Panel Session:** "Test Challenges of 3D-Stacking Structures", Panel Chair: Gene Atwood (IBM); Organizer: Yu Huang, Mentor Graphics
Thursday, May 10	
	Registration
7:00 - 8:00 am	**Breakfast**
8:00 - 8:15 am	**Opening Remarks:** Paul Reuter, *General Chair*
8:15 - 9:00 am *Introduction by Martin Margala, Program Co-Chair*	**Keynote Address:** "Opportunities and Challenges in the Design and Test of Post-CMOS Memories" by Dr. Fabrizio Lombardi, Northeastern University **Abstract:** This talk will present new developments in the design and test of memories using post-CMOS technologies. The MOSFET as basic device for CMOS implementation is fast moving in the deep nanometric scales (well below 45 nm), and its limitations for memory circuit design are starting to become evident, as reflected by the presence of soft errors, power management and volatility. Moreover new memory paradigms are being sought and emerging in a variety of applications. Among them, multi-level storage and non-volatile operation are very compelling features. New materials and physical phenomena have been proposed and utilized for commercially meeting these challenges, thus affecting circuit design, defect modeling and ultimately testing.This talk will outline some of these new technologies (such as based on phase change and memristance); trends, obstacles and possible solutions for the design and test of these memories will be presented and discussed.
9:00 - 9:45 am *Introduction by Martin Margala, Program Co-Chair*	**Invited Address:** "Data Analytics and Applications for End-to-End Optimization" by Matthias Kamm**,** Cisco **Abstract:** Yield is typically optimized in a given plant; fabrication plant, test floor, or contract manufacturer. To optimize end-to-end yields new models of cooperation, sharing and data analysis are required. Optimization can also focus on cost and quality depending on the end product. Certain types of device IP such as electronic chip ID, and new test standards such as the upcoming P1687 can also facilitate these improvements.
9:45 - 10:10 am	**Coffee Break / Reception**
10:10 - 11:30 am	**Student Session 1 Fault Tolerance, Error Resilience and Validation**
	Dimitry Burlyeav(TUDelft, NL): SystemC-based On-board Computer Modeling for Design Fault-Tolerance Assessment *Adrian Mocanu(PolitecnicaU, Romania)*: Using ANOVA to validate the accuracy of a simulation *Suraj Sindia(AuburnU, US)*: Optimizing Fault Coverage for Error Resilient Applications: An Integer Linear Programming Formulation
11:30 - 12:00 pm	**Break**
12:00 - 1:00 pm	**Lunch**
1:00 - 2:00 pm	**Student Session 2 BIST**
	Preet Jain(SVITS, India): BIST for System on Chip (SoC) for Biomedical Signal Processing *Samed Maltabas(UMassLowell, US)*: A New Built-In IDDQ Test Flow For PLLs Using Programmable Built-In Current Sensor

2:00 – 2:15 pm	**Break**
2:15 - 3:15 pm	**IEEE Women in Engineering Session:** Session Chair: Denise Griffin, WIE Boston Chair
	Samantha Pham(SMU, US): An Analysis of Differences between Trojans inserted at RTL and at Manufacturing with Implications for their Detectability *Dimitra Papagiannopoulou(BrownU, US)*: Flexible Data Allocation for Scratch-pad Memories to Reduce NBTI Effects *Farhana Rashid(AuburnU, US)*: Using Weighted Random and Transition Density Patterns for BIST
3:15 - 3:30 pm	**Break**
3:30 – 4:10 pm	**Student Session 3 Analog and Mixed-Signal Test**
	Kemal Kulovic(UMassLowell, US): Flexible VITAL Embedded Instruments For Built-In Test of AMS Power SOCs *Osman Ekekon(UMassLowell, US)*: Comparison of On-Chip Measurement Techniques for Second Order Phase Locked Loop Performance Metrics
4:10pm – 6 pm	**Break**
6 pm – 8 pm	**Banquet and Best Student Paper Award**
Friday, May 11	
	Registration
7:30 - 8:00 am	**Breakfast**
8:00 - 8:45 am	**Friday Keynote Address:** "Timing Tests in the Face of Random Transistor Performance Variability" by Prof. Adit Singh, Auburn University **Abstract:** As technology scales, resistive defects, particularly via voids and gate oxide failures, can occur with increasing frequency. While such defects may initially only cause a small timing increase along some signal paths during test, in time they can grow and lead to early life failures in the field. Testing for small delay defects is therefore receiving considerable attention, particularly because the traditional burn-in approach to screen out such infant mortality failures is becoming extremely expensive in highly scaled nanometer technologies. Unfortunately, random process variations can also give rise to variability in circuit timing comparable to the resistive delay faults being targeted. This can mask the detection of reliability defects during test. Screening out all suspect parts can lead to excessive yield loss. In this talk, we explore this challenge in the context of scan based delay testing, and offer some innovative solutions to this difficult problem.
8:45 – 8:55 am	**Break**
8:55 - 10:10 am	**Session: Special Session on Solid-State Circuit Test and High Availability Systems,** Session Chair: Pascal Nsame *Timothy Platt(IBM)*: Computing EVM in Real Time for Wireless Communication Test *Eli Brookner(Raytheon)*: Achievement & Future Trends in Phased Arrays & Radars; Test Impact of Scaling to 11nm *Pascal Nsame(IBM)*: Product Soft Fails in High Availability Systems and Test Implications
10:10 - 10:20 am	**Break**
10:20 - 12:00 pm	**Paper Session Industrial Test Practices**
	Jianbo Li(TsinghuaU, China, Mentor, US): A Hybrid Flow for Memory Failure Bitmap Classification *Robert Seitz(AMS, Austria)*: Release to Production *Ranjit LoboPrabhu(Netronome, US, Cadence, US)*: Distributed Parallel Test Architecture *Brion Keller(Cadence, US)*: DfT Insertion and Interconnect Test Generation for 3D Stacks with JEDEC Wide-IO DRAM
12:00 - 1:00 pm	**Lunch and Program Committee Meeting**
1:00 - 2:15 pm	**Paper Session Scan Test**
	Jing Ye(TsinghuaU, China, Mentor, US): Diagnosis Aware Scan Chain Reordering *Wu Yang (Mentor, US)*: Industrial Practices for Silicon Debug of Scan Based Designs *K. Chakravadhanula(Cadence, US)*: Smartscan - Reduced Pin Count Compression with Low Power Advantages
2:15-2:20 pm	**Closing Remarks**, Paul Reuter